REMARKS

Reconsideration of the present application is respectfully requested.

The rejection of claim 1 under 35 USC 103(a) as being unpatentable over Bowes et al. in view of Gittinger et al. is respectfully traversed.

When the references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. The motivation to combine references may come from the references themselves, from knowledge of those skilled in the art that certain references are known to be of interest in the particular field, or from the nature of the problem to be solved.

The Office Action has not provided any objective evidence of record to show a motivation to combine the applied references. The Office Action provides only the following statement – not evidence – to support the alleged motivation to combine the references: "Given the teaching of Gittinger, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-know or conventional feature of the method, such as taught by Gittinger, in order to provide reducing the burden on the primary processor."

That statement is entirely conclusory. No reference, affidavit or other objective evidence is provided in the record that supports that one skilled in the art, considering how to reduce the burden on the primary processor, would arrive at using the claim 1 feature retrieving a first portion of the recorded data via the bus and updating some of the registers via the bus. This lack of objective evidence prevents making a *prima facie* case of obviousness for claim 1. Therefore, since there is no sufficient objective evidence of record that shows a motivation to combine the applied references as contended by the Office Action, claim 1 is not obvious and is allowable.

Moreover, that conclusory statement is incorrect. Bowes et al. relatedly disclose "DMA is achieved through a DMA controller which manages the transfer, thereby alleviating the central processing unit (CPU) of the task." Col. 1, lines 29-31. In light of that disclosure, one skilled in the art would use a DMA to reduce the burden on the primary processor. This objective evidence contradicts the Office Action's contention that one skilled in the art, considering how to reduce the burden on the primary processor, would arrive at using the claim 1 feature retrieving a first portion of the recorded data via the bus and updating some of the registers via the bus. Thus, there is no motivation shown of record to combine these two references.

The rejection of claims 2-5 under 35 USC 103(a) as being unpatentable over Bowes and Gittinger, and further in view of Cloke is respectfully traversed.

Claims 2-5 depend from claim 1. Claim 1, as explained above, is not obvious. Cloke does not overcome deficiency of those references. Therefore, claims 2-5 are allowable due to their dependence on allowable claim 1.

The rejection of claims 6, 8, 9, 11-20 under 35 USC 103(a) as being unpatentable over Bowes et al. in view of Cloke is respectfully traversed.

Claim 6 features retrieving via the DMA controller several values. The Office Action contends that this step is shown in Bowes et al. at col. 5, lines 42-65. This contention is erroneous. That cited disclosure states "using the values in its active register set." Those values are set by the CPU (see Fig. 3, reference number 260). Therefore, the DMA is not retrieving values; instead the CPU is program the "active register set." This step, then, is not taught by Bowes et al. And Bowes et al. nowhere suggest this step.

Cloke does not overcome this lack of teaching or suggestion. Cloke explicitly discloses that "[m]icroprocessor 34 can update the channel parameters." See col. 27, lines 57-58. Thus, Cloke, like Bowes et al., does not teach this claim feature of retrieving via the DMA controller several values. Similar to the teachings of Bowes et al., the DMA is not retrieving values; the CPU is programming the active register set. And Cloke nowhere suggest this step. Thus, claim 6 is not obvious and is therefore allowable.

For an entirely different reason claim 6 is not obvious. The Office Action has not provided any objective evidence of record to show a motivation to combine the applied references. The Office Action provides only the following statement – not evidence – to support the alleged motivation to combine the references: "Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-know or conventional feature of the method, such as taught by Cloke, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disc surface."

That statement is entirely conclusory. No reference, affidavit or other objective evidence is provided in the record that supports that one skilled in the art, considering how to maintain disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disc surface, would arrive at the invention of claim 6. This lack of

objective evidence prevents making a *prima facie* case of obviousness for claim 6. Therefore, since there is no sufficient objective evidence of record that shows a motivation to combine the applied references as contended by the Office Action, claim 6 is not obvious and is allowable. Claims 8, 9, 11-14 are also allowable for the same reasons explained for claim 6.

Claim 15 features the bus controllable by the DMA controller to update several of the registers.

The Office Action contends that this step is shown in Cloke at col. 27, line 55 to col. 28, line2. This contention is incorrect. Cloke explicitly discloses that "[m]icroprocessor 34 can update the channel parameters." See col. 27, lines 57-58. This is not identical to the claim 15 feature of the bus controllable by the DMA controller to update several of the registers. And Cloke does not suggest such a feature.

Bowes et al. do not overcome this Cloke deficiency. Bowes et al. disclose "using the values in its active register set." Those values are set by the CPU (see Fig. 3, reference number 260). Bus 260 is not controllable by the DMA controller to update several of the registers. Instead, it is controlled by the CPU. This feature, then, is not taught by Bowes et al. And Bowes et al. nowhere suggest this feature. Thus, claim 15 is not obvious and is therefore allowable.

For an entirely different reason claim 15 is not obvious. The Office Action has not provided any objective evidence of record to show a motivation to combine the applied references. The Office Action provides only the following statement – not evidence – to support the alleged motivation to combine the references: "Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-know or conventional feature of the method, such as taught by Cloke, in order to provide reducing the burden on the primary processor."

That statement is entirely conclusory. No reference, affidavit or other objective evidence is provided in the record that supports that one skilled in the art, considering how to provide reducing the burden on the primary processor, would arrive at the invention of claim 15. This lack of objective evidence prevents making a *prima facie* case of obviousness for claim 15. Therefore, since there is no sufficient objective evidence of record that shows a motivation to combine the applied references as contended by the Office Action, claim 15 is not obvious and is allowable.

The basis for the rejection of claim 16 is unclear. The Office Action states:

Claim 16 is directed to a method of implementing the storage system as set forth in claim 1. Since Bowes and Cloke teach the storage system as set forth in claim 1; therefore, they also teach the method as set forth in claim 16.

The combination of Bowes and Cloke was not asserted against claim 1. Since that was not done, the specifics of this claim 16 rejection using Bowes and Cloke are unknown. Without the specifics, the issues regarding this rejection are not known. As a result, the Applicant cannot meaningfully respond to this rejection. Applicant therefore respectfully requests the specifics of this rejection in the next Office Action. That next Office Action should not be made final because no specifics were given for this rejection. Because of this, the rejections of claims 17-20 are also unclear.

The rejection of claims 7 and 10 under 35 USC 103(a) as being unpatentable over Bowes et al. and Cloke in view of Asakawa et al. and Machado et al., respectively, is respectfully traversed.

Claims 7 and 10 depend from claim 6. As explained above, claim 6 is not obvious in view of Bowes and Cloke. Neither Asakawa et al. nor Machado et al. overcome the deficiency of Bowes and Cloke. Thus, claim 6 is not obvious in view of the two additional references. As such, claims 7 and 10 are also not obvious, and are allowable.

As explained above, all the pending claims are patentable over the applied references. The examiner is respectfully requested to allow all the pending claims and new claims 16-20, and pass this case to issuance.

Respectfully submitted,

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(Assignee of Entire Interest)

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Date

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